6.8 A Sub-1mm² Dynamically Tuned CMOS MB-OFDM 3-to-8GHz UWB Receiver Front-End

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Ultrawide Band (UWB) Multi-Band OFDM (MB-OFDM) systems have been proposed as an emerging solution to wireless communication applications requiring high data rates (up to 400Mb/s) over short distances [1]. In one proposed version, the modulated carrier with a bandwidth of 528MHz can hop to one of fourteen channels ($2904 + 528 \cdot n$MHz, n = 1, 2…14), divided into four groups of three channels and one group of two channels. To assure the widest possible adoption, RF portions of these systems should consume little dc power and die area, and be implemented in a standard CMOS process. These last requirements argue against the use of on-chip inductors wherever possible.

A dynamically tuned UWB OFDM receiver front-end is presented in a 0.18µm CMOS technology. The receiver uses no on-chip inductors and consists of a dynamically tunable low-noise amplifier (LNA), a downconverter and a tunable intermediate frequency (IF) bandpass filter. The receiver is designed to work for the lower three groups; however, the concept can easily be extended to include the higher groups.

A direct-conversion UWB receiver, while attractive for power consumption and simplicity of local oscillator (LO) scheme [2], has the well-known problems of time varying dc offset and sensitivity to narrowband jammers. Since the LO can vary from 3.5 to 10.3GHz, the dc offset present at the mixer output can vary significantly with every frequency hop, and the offset calibration loop has to settle to its final value well within the guard interval of 9ns. A differential heterodyne architecture largely eliminates the dc offset issues and provides the additional advantage of reduced second-order distortion, reducing the dc power requirements. One of the drawbacks of a heterodyne receiver; the need for an interstage filter, has been overcome in this design by creating a passive band-pass filter entirely with bond wires and on-chip capacitors.

To avoid the classical heterodyne receiver image rejection problem, the frequency plan was carefully designed for an IF of 2.64GHz, so that all the images fall below 2.4GHz. An external bandpass filter with a lower cut-off frequency of 3GHz, which is standard in UWB receiver designs, therefore suppresses all the images, as shown in Fig. 6.8.1. In addition, the LNA provides some image rejection, eliminating the need for an image reject mixer.

The LNA (Fig. 6.8.2) is a differential cascode amplifier (to enable operation at 2.3V without breakdown) with an *LC* load. To eliminate the use of on-chip inductors, the load is realized with bond wires and on-chip capacitors. Input matching is achieved via resistive feedback and optimized device sizing. The output device capacitance and mixer input capacitance resonate with the bond wires at 7GHz. The tank's Q is then reduced by a shunt resistor, broadening the bandwidth of the circuit. This provides for good LNA gain in Group 3 (6.3 to 7.9GHz). When the received signal is in the lower-band Group 2 or Group 1, extra shunt capacitance is switched in, by setting bits b_0 and b_1 "high" successively, to dynamically maximize the gain of the LNA at 5.5GHz and 4GHz. Dynamic tuning, in addition to rejecting the images below 2.4GHz, attenuates "out-of-group" signals, which may create intermodulation products at the desired channel.

The mixer is a wideband, double balanced Gilbert-Cell based mixer. The LNA provides for a minimum of 7dB of image rejection and further image suppression is obtained by the external bandpass filter before the LNA. The mixer, therefore, does not need to provide any additional image rejection.

Since there might be multiple MB-OFDM transmitters operating in the vicinity, it is necessary to provide for some on-chip IF channel selection to ease linearity requirements on the rest of the receive chain and eliminate the need for an external IF filter. Unfortunately, active filters have well known dynamic range and power limitations, and an on-chip *LC* filter would require high-Q inductors and significant die area. The goal of this design is to keep the area as small as possible, while maintaining adequate performance. An impedance inversion transformation was applied to a standard single-ended 3rd-order passive bandpass Chebyshev filter, resulting in a "top-C" coupled structure, with fixed equal-valued shunt grounded inductors. The downbond inductance for our package was determined to be 0.8nH and the capacitor values were chosen appropriately. The final differential filter is shown in Fig. 6.8.3. The filter was designed for an IF center frequency of 2.64GHz, a bandwidth of 528MHz, and is tunable by ±300MHz via independently tunable varactors. This tuning range covers a ±20% variation in capacitance and ±10% variation in bond wire length, which is typical. The 2dB drop in gain at the band edges has a small effect, since the ten carriers at the band edge are guard carriers. A potential problem with this filter is the possibility of noise coupling onto the bond-wires. But since the receiver has almost 20dB of gain before the filter, this is not a significant issue.

The final measured results for the chip in an MLF24 package are shown in Figures 6.8.4 through 6.8.6 and the active area is only 0.35mm² in a 0.18µm CMOS process. Fig. 6.8.4 shows the measured receiver response for various channels. The receiver gain varies between bands, with the gain decreasing slightly at the lower bands due to the switch loss. This gain variation is not a significant system issue, since the received signal strength will also vary over frequency (with the most likely scenario being decreased signal strength at the higher frequencies).

The receiver achieves a 5 to 6.5dB noise figure across all the bands, -2.6dBm input IP3 and +33dBm input IP2, while drawing only 19.5mA from a 2.3V supply. The receiver could operate at a supply voltage as low as 1.5V if a passive mixer was employed, at the expense of a slightly higher noise figure. The gain variation across each channel is typically 2.5dB. Compared to a standard wideband receiver design, this architecture offers the advantage of smaller die area, simpler design, no external components and dynamic rejection of out-of-group jammers. The receiver uses no on-chip inductors or any other off-chip matching components, and is therefore an attractive approach for a highly integrated receiver in a standard CMOS process.

Acknowledgements:
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References:
[1] Anuj Batra et al., "Design of a Multiband OFDM System for Realistic UWB Channel Environments," *IEEE T. Microwave Th. and Tech.*, vol. 52, no. 9, p. 2123-2138, Sept., 2004.
[2] A. Ismail and A. Abidi, "A 3.1 to 8.2 GHz Direct Conversion Receiver for MB-OFDM Communications," *IEEE ISSCC Dig. Tech. Papers*, pp. 208-209, Feb., 2005.

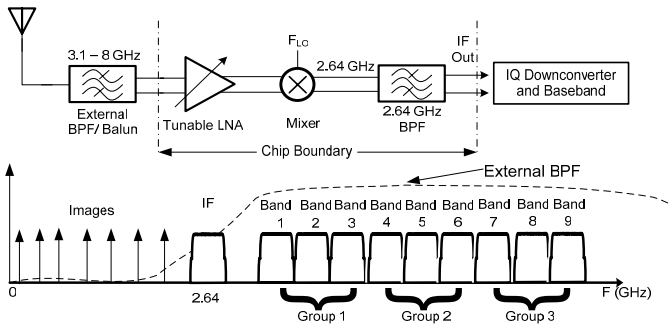

Figure 6.8.1: Receiver architecture and frequency plan.

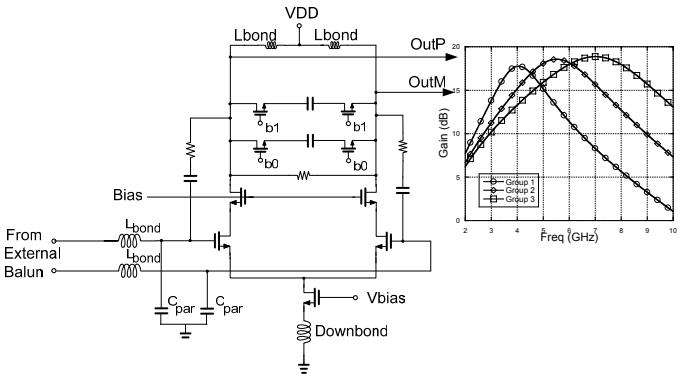

Figure 6.8.2: Low noise amplifier schematic and simulated frequency response.

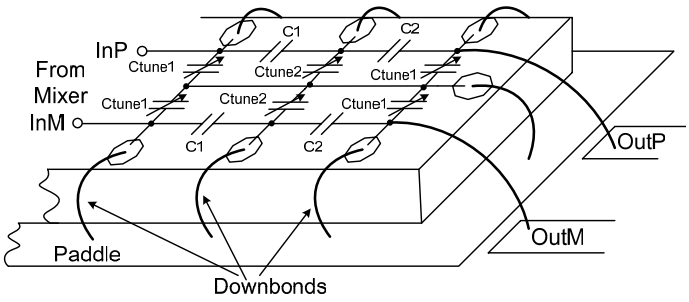

Figure 6.8.3: Differential band-pass filter.

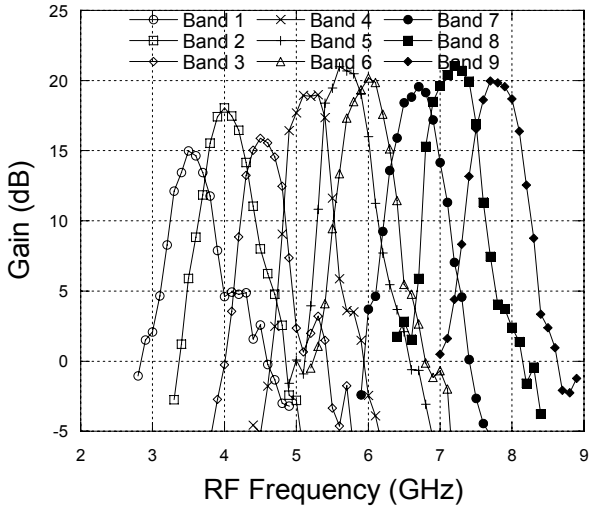

Figure 6.8.4: Measured receiver gain in each band.

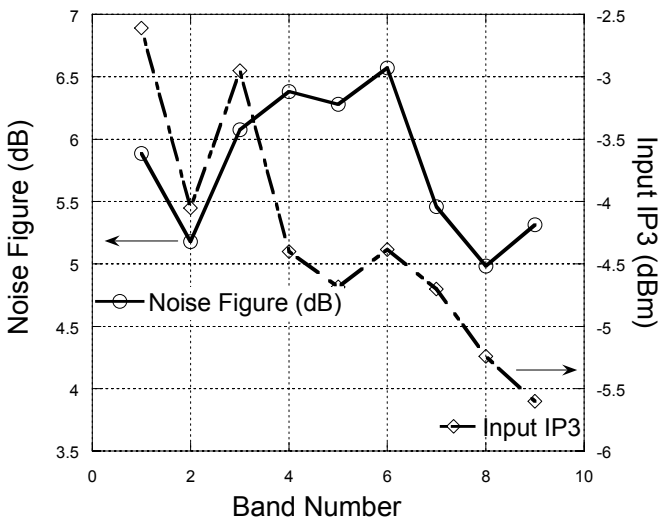

Figure 6.8.5: Measured receiver noise figure and input IP3.

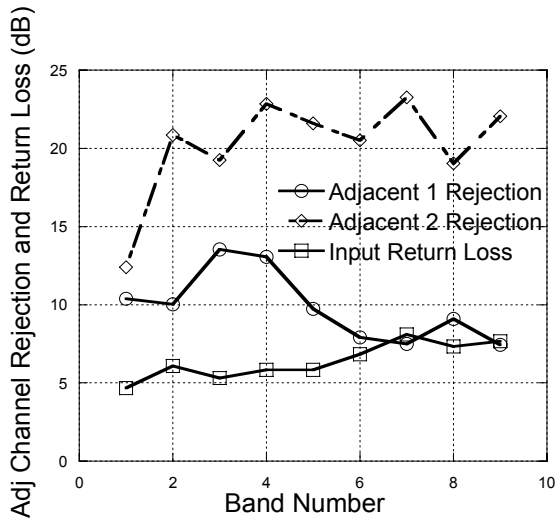

Figure 6.8.6: Measured adjacent channel rejection and input return loss.